Design An X-Band Frequency Synthesizer

H. Ameri, A. Attaran, M. Moghavvemi

Department of Electrical Engineering, Faculty of Engineering, University of Malaya, Kuala Lumpur 50603, Malaysia

Microwaves & RF, vol. 49, pp. 98-103, June 2010.

Abstract: This frequency synthesizer design aims at achieving low phase and high reliability for X-band digital microwave radio applications, using a commercial device and frequency tripling techniques.

Digital microwave radio (DMR) applications require frequency sources with stable outputs and low phase noise. One possible solution is an Xband frequency synthesizer designed for use from 7.7 to 8.2 GHz. It is based on multiplying by three a reliable source operating from 2.56 to 2.74 GHz with outstanding phase-noise performance to achieve final output signals with -84 dBc/Hz phase noise offset 10 kHz from the carrier. The prototype synthesizer features a large tuning voltage range and low operating voltage requirements.

Low phase noise is critical to many wireless systems and radar.[1] An X-band frequency synthesizer, for example, in addition to supporting DMR systems, can be multiplied and mixed with local oscillator (LO) signals to cover multiple- frequency applications through 65.6 GHz.[2]

A variety of synthesizer architectures, such as direct-digital, direct-analog, and indirect-synthesis techniques can be used in modern transceivers, although they each have tradeoffs. Direct-analog synthesizers feature the lowest phase noise with fast switching speed, using mixers to translate the frequencies of surface-acoustic-wave (SAW), coaxial-resonator-oscillator (CRO), dielectric-resonator-oscillator (DRO) and other lower-frequency sources. Unfortunately, direct-analog synthesizers are complex and expensive to design.[4] A DDS approach is not suitable for wideband frequency generation since it follows Nyquist criteria, with a maximum frequency that is less than one-half that of the sampling frequency of a digital-to-analog converter (DAC). A DDS provides high frequency resolution and fast switching speed for reasonable cost, but with poor spurious performance.

Phase noise can determine the sensitivity of a receiver in the presence of an adjacent signal. For radar systems susceptible to noise offset 10 kHz from the carrier, the phase noise of a VCO is the dominant source of noise. One way to reduce phase noise is by reducing the bandwidth, although this is not an option for applications requiring wide bandwidths. A divide-by-N module raises the phase noise of the initial frequency source since the signal and noise are both multiplied by N. For optimum phase noise, a synthesizer's loop filter bandwidth must be wide enough to reject VCO noise. Because of the high phase noise from a divide-by-N module, replacing it with a

multiplier module can improve phase noise.5 Although frequency resolution will be compromised as a result, fine resolution can be achieved by means of a direct-digital-synthesizer (DDS) module. The inherent high spurious levels of the DDS module can be reduced by means of bandpass filtering.

There are many ways to assemble a wideband frequency synthesizer with phase-lock-loop (PLL) integrated circuits (ICs), narrowband frequency synthesizers, mixers, and multipliers. Mixing and multiplying are the most common methods for designing microwave and millimeter-wave frequency synthesizers not plagued by loop limitations. In a multiplier module, for example, the input frequency is multiplied by an integer coefficient to produce a higher output frequency. Although multiplication results in phase-noise degradation, a typical method of producing high-frequency synthesizers with wide output bandwidths is by multiplying a fixed-frequency or narrowband low-frequency synthesizer. In a mixer frequency-synthesizer structure, the output phase noise will be 3 dB/Hz higher than the highest phase noise of the two mixed modulus sources:

$$PN_{\text{after multiplication}} = PN_{\text{before multiplication}} - 2\log(\text{mult. coefficient}) \quad (1)$$

Mixer techniques can also be used to create wideband synthesizers. The input frequency and LO frequency are added and subtracted, with highpass filtering removing spurious products.

Many frequency synthesizers are based on the use of PLLs, where a frequency divider module divides the output frequency by integer 1, as shown in ***Fig. 1*** and Eq. 2:

$$F_{output} = F_{input} \times N \quad (2)$$

A PLL synthesizer can generate several frequencies within the bandwidth of the VCO by constant frequency spacings from $F_{reference}$ as explained in ref. 5. A linear model of a PLL synthesizer is a closed-loop system with a number of different phasenoise sources as shown in Fig. 1[7]:

$$H(S) = F_{in}(S)/F_{out}(S) = [K_{PFD}K_{VCO}\text{-}G_{loop\ filter}(S)]/[s + K_{PFD}K_{VCO}G_{loop\ filter}(S)] \quad (3)$$

Assuming the loop filter is first order:

$$G_{loop\ filter}(S) = 1/[1 + (s/\omega_{LPF})] \quad (4)$$

Substituting Eq. 4 into Eq. 3 creates:

$$H(S) = (K_{PFD}K_{VCO})/[(s^2/\omega_{LPF})+s + K_{PFD}K_{VCO}] \quad (5)$$

While the VCO and loop filter are first order, the system is second order.

Figure 2 shows an example of the multiplying technique, where output signals are required from 7.7 to 8.2 GHz with phase noise of -84 dBc/Hz offset 10 kHz from the carrier. With a ×3 multiplier, the characteristics calculation is as (7.68 – 8.20)/3 = 2.56 – 2.74 GHz with -94 dBc/Hz phase noise required for the 2.56-to-2.74- GHz bandwidth:

$$-84 - 20\log(3) = -94 \text{ dBc/Hz} \quad (6)$$

The step size of the primary synthesizer is 10 kHz, with the final multiplied step size expressed as:

$$\text{Step size}_{7.7\text{-}8.2\ \text{GHz}} = 10\ \text{kHz} \times 3 = 30\ \text{kHz} \quad (7)$$

A PLL frequency synthesizer's building blocks include a reference frequency source, loop filter, phase/frequency detector (PFD), and divide-by- N modules.[6] The loop filter is the most critical module since it affects the inband phase noise (from the reference oscillator) and helps eliminate spurious and adjacent harmonic frequencies. The loop filter must also provide adequate control voltage for the VCO. Passive filters provide about 5 V, while active filters support from about 0 to 22 VDC. In the block diagram (***Fig. 1***), divider N reduces the VCO's frequency to F_{VCO}/N. The PFD detects the difference between an input frequency and the frequency of the VCO (F_{VCO}) divided by integer N (F_{VCO}/N) and, based on the phase or frequency difference, generates a DC voltage to tune the VCO.

In a PLL, the VCO is the dominant source of phase noise (***Fig. 3***):

$$\text{Open loop gain: } G_{OL}(s) = K_{PFD}G_{\text{loop filter}}(S)K_{VCO}(1/S) \quad (8)$$

To minimize phase noise, the phase detector gain, K_{PFD}, should be maximized to minimize the sensitivity of VCO gain, K_{VCO} [8,9]:

$$\Delta F_{out}/V_{control} = (1/K_{PFD})\left(N/\{1 + [1/G_{OL}(s)]\}\right) \quad (9)$$

$$\Delta F_{out}/V_{control} = (K_{PFD}/s)/[1+G_{OL}(s)] \quad (10)$$

Flicker noise expresses close-in noise[8]:

$$S_\theta(f_m)=(F_{KTB}/P_{avs})(1+f_c/f_m) \quad (11)$$

where
F = noise value expression,
K = Boltzmann's constant,
T = environment temperature,
B = bandwidth (usually 1 Hz),
Pavs = the loop output power,
Fc = center frequency,
fm = offset frequency,
1/N = divider ratio,
KPFD = phase detector transfer function,
H(s) = loop filter transfer function, and
KVCO = VCO transfer function represented in Eq. 7.

Referring to Fig. 1, the transfer functions of the noise sources from reference oscillator to output is

$$H_{ref}(s) = F_{out}(s)/\Delta F_{ref}(s) = N/[1+ 1/G(s)] \quad (12)$$
$$H_{PFD}(s)=F_{out}(s)/\Delta F_{PFD}(s)=N/[1+ 1/G(s)] \quad (13)$$
$$H_{VCO}(s) = F_{out}(s) /\Delta F_{VCO}(s) = N/[1 + 1/G(s)] \quad (14)$$

Overall synthesizer phase noise is calculated as

$$L_{out}(f_{out}) = 10\log\{\log^{-1}[N_{VCO}(f)/10] + \log^{-1}[N_{ref}(f)/10] + \log^{-1}[N_{filter}(f)/10] + \log^{-1}[N_{PDF}(f)/10]\} \quad (15)$$

where

$$N_{PFD}(f) = L_{PFD}(f_{out}) + 20\log[|N/H_{PFD}(s)|] + 20\log N \text{ (dBc/Hz)} \quad (16)$$
$$N_{ref}(f) = L_{PFD} + 20\log[|N/H_{ref}(s)|] + 20\log N \text{ (dBc/Hz)} \quad (17)$$
$$N_{VCO}(f) = L_{VCO}(f_{out}) + 20\log[|1 + 1/G(s)|] \text{ (dBc/Hz)} \quad (18)$$
$$N_{filter}(f) = 20\log[|N/[(2)^{0.5}K_{PFD}|G_{filter}(s)|\,|1 + 1/G(s)|] + 20\log N \text{ (dBc/Hz)} \quad (19)$$

The noise source transfer function of each block responds to the equations above. Each has G(s)/[1 + G(s) H(s)] in common. This is called the in-band noise relation where ?c is the loop bandwidth, f_c is the loop phase, and H(s) is the feedback loop gain, $1/N$[10] :

$$|G(j\omega_c)H(s)| = 1 \quad (20)$$
$$\theta_c = 180 - \angle G(j\omega_c)H(s) \quad (21)$$

Note that G(s) has a reverse relation with s or ?c as shown in ***Fig. 4*** and Eq. 22:

$$G(s)/[1 + G(s)H(s)] \approx \begin{cases} N & \omega \ll \omega_c \\ G(s) & \omega \gg \omega_c \end{cases} \quad (22)$$

To validate these assumptions on phase noise, the Advanced Design System (ADS) software from Agilent Technologies was used to simulate performance at 2.7 GHz (***Fig. 5***). For further validation, a frequency synthesizer for 2.50 to 3.0 GHz (***Fig. 6***) was designed using the ADISimPLL software from Analog Devices. The circuit has a model ADF4108 synthesizer integrated circuit (IC), a model OP484 opamp IC from Analog Devices, and model HMX-333-16D VCO IC from Z-Communications (). A model RMK-3-123+ multiplier from Mini-Circuits was used for the integer 3 multiplication. Simulation results show phase noise of -99 dBc/Hz offset 10 kHz from a 2.7-GHz carrier, which agrees with ADISimPLL simulation results in the table. Simulations show the first three spurious frequencies at -46, -67, and -80 dBc, primarily from reference spurs. The step size and loop bandwidth relationship indicates the spur attenuation level. The spacing between the first three spurs is usually equal to the step size or one-half of the channel step size. A step size of 25 kHz and loop bandwidth of 15 kHz were chosen to optimize spurious levels.

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